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| EXAMINER | |
|---|---|
| FENNEMA, ROBERT E | |
| ART UNIT | PAPER NUMBER |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/665,290 | SODERQUIST ET AL. | |
| | Examiner | Art Unit | |
| | ROBERT E. FENNEMA | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-7 and 10 have been considered. Claims 1 and 10 amended as per Applicant's request.

### *Claim Objections*

2. Claims 2-7 and 10 are objected to for referring to "A" digital signal processor. "A' should be replaced with "The" to make clear that the claims are referring back to the same DSP as in the independent claim, as opposed to a different one (which would create possible 112 issues if it was the case).

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Dhuey (USPN 5,768,602).

5. As per Claim 1, Dhuey teaches: A digital signal processor comprising:

an instruction memory (Column 1, Line 44, the hard drive), a central arithmetic unit (Column 2, Lines 35-36, a central arithmetic unit is required in a computer, especially to perform audio and video processing), a register (inherent in a computer), a

controller (Column 4, Lines 10-13, the sleep mode controller), an event control unit (Column 8, Line 64 – Column 9, Line 2, the Power manager) and input/output devices (Column 2, Line 35);

the instruction memory is arranged to include operation code including logical operations (Required in a computer, but also see Column 2, Lines 33-35, the non-real time instructions), time performance constraints (Column 4, Lines 54-56, doze mode) and events (Column 9, Lines 28-30, the exiting of sleep mode (in sleep mode, as shown in Column 5, Lines 54-56, the clock is slowed down, thus being a time performance constraint));

the controller is arranged to suspend all further processing of the time performance constraints after initiating operations in an event control unit (Column 9, Lines 27-30 and 5-19, when sleep mode is exited, the time performance constraints (sleep mode) is suspended) and resume processing when advised by the event control unit (Column 5, Lines 54-56 and Column 8, Line 64 - Column 9, Line 2, when sleep mode is reactivated, the time constraints come back);

the event control unit is arranged to recognize an event and in response to the detection of the event execute a processing operation and initiate or resume processing of the controller upon completion of the processing operation, wherein the event is an input signal or a completion of processing from a previous event (Column 9, Lines 38-43) and the operation code comprises an event operand arranged to identify the input signal or previous event to initiate or resume processing of the event control unit (Column 9, Lines 38-43, the test instruction has an operand) and a delay operand

comprising those time performance constraints (Table 2) executed by a counter in the event control unit (Column 8, Lines 66-67, a passage of time can control the event controller, which requires a counter).

6. As per Claim 2, Dhuey teaches: A digital signal processor in accordance with claim 1, wherein the event is detected by the event control unit (Column 9, Lines 39-50, the Power Manager looks for both event beginnings and ends).

7. As per Claim 3, Dhuey teaches: A digital signal processor in accordance with claim 2, wherein the event control unit is arranged to detect input signals (Column 9, Lines 45-47).

8. As per Claim 4, Dhuey teaches: A digital signal processor in accordance with claim 2, wherein a further event is recognized as a completion of the processing carried out as a consequence of a previous event (Column 9, Lines 45-47, the “time to sleep or wake” is based on the completion of an event).

9. As per Claim 5, Dhuey teaches: A digital signal processor in accordance with claim 1, wherein the event is recognized as a completion of the processing carried out as a consequence of a previous event (Column 9, Lines 45-47, the “time to sleep or wake” is based on the completion of an event).

10. As per Claim 6, Dhuey teaches: A digital signal processor in accordance with claim 1, wherein the event control unit includes a signal memory arranged to store and extract data under control of the event control unit (Column 9, Lines 38-43, the memory is where the condition is stored, which must be somewhere).

11. As per Claim 7, Dhuey teaches: A digital signal processor in accordance with claim 6, wherein the signal memory is a vector memory (Column 2, Line 27).

12. As per Claim 10, Dhuey teaches: A digital signal processor in accordance with claim 1, including two or more event control units arranged to work independently from each other (Column 8, Line 64 – Column 9, Line 2, multiple units exist that can trigger events).

### *Response to Arguments*

13. Applicant has argued that Dhuey does not teach a controller suspending all further proceeding of time performance constraints after initiating operations in the event control unit, and argues that Dhuey is geared towards changing the clock speed. However, Examiner believes that this is an appropriate mapping to the claim, as "time performance constraints" is an incredibly broad limitation, which Examiner has interpreted as anything that has to do with the timing of the processor, which clock speed would certainly fit into. The time performance constraints are the system operating at normal speed, when the event signals entering sleep mode, the time

performance constraints are no longer carried out, because the clock was slowed down. When the system wakes up, the clock speed goes back to normal, thus processing the "time performance constraints". The length of time that the system is in these modes can be set by a value using a counter (delay operand comprising time constraints executed by a counter), see Column 9, Lines 39-43. Given that these teachings appear to fit within the claim limitations present, Examiner believes that the rejection is proper.

14. Examiner has several suggestions on how to amend the claims to overcome the reference, primarily focusing around being more specific on some of the more vague limitations, primarily the time performance constraints. In fact, Examiner suggests entirely removing the language of “time performance constraints”, and replacing it with something that more clearly indicates what is being claimed, for example, a "delay operand" as described on Page 4 of the specification (as opposed to the delay operand currently claimed, which does not give very much information as to what it is, other than having something to do with time performance constraints), or rather than claiming the very broad and somewhat confusing "time performance constraints", giving it a definition, or claiming said definition (as long as it is supported by the specification). Ultimately, to overcome the reference, Examiner believes it needs to be made very clear what is being suspended by the event control unit. Is it an instruction, is it a mode, is it an operand for an instruction, is it real time processing, it's not clear, and as a result, the broadest reasonable interpretation is any of those (mode in this case).

Examiner believes that clarifying "time performance constraints" would almost certainly overcome Dhuey.

15. If Applicant wishes to discuss any issues with the case with the Examiner, the Applicant is welcome to contact the Examiner for an interview at the phone number listed at the end of this action.

***Conclusion***

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

17. Bonola (USPN 5,913,058) teaches an event to enable and disable a real-time clock to prevent real-time interrupts during certain modes of processing.

18. Owen et al. (United States Patent Application Publication 2004/0088704) teaches a system which disables all non-real time interrupts in real time mode.

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT E. FENNEMA whose telephone number is (571)272-2748. The examiner can normally be reached on Monday-Friday, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

Robert E Fennema
Examiner
Art Unit 2183

RF